High Efficiency, Wide Dynamic Range Variable Gain and Power Amplifier MMICs for Wide-Band CDMA Handsets

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***Abstract*—A linearized variable gain amplifier (VGA) and a two-stage power amplifier (PA) MMIC were developed for 1.95-GHz wide-band CDMA (W-CDMA) handsets application. A complete PA block with power control ability was obtained by cascading the VGA with the PA. The linearized VGA consists of a predistorter (PD) integrated with a conventional VGA, performing dual function for achieving high linearity power control, as well as reducing output distortion level of the following PA. With the use of predistortion, the $P_{\rm out}$ and power added efficiency (PAE) of the PA block improved from 27.5 dBm and 39.8% to 28.5 dBm and 44.8%, respectively, measured at −35 dBc adjacent channel leakage power ratio (ACPR). Under power control operation, the control range of the PA block increased from 23.6 dB to 31.2 dB, and ACPR reduction of over 10 dB was achieved with the use of linearized VGA.**

***Index Terms*—High efficiency, linearization, linear power amplifier, MMIC, predistortion.**

I. Introduction

WIDE-BAND CDMA (W-CDMA) is emerging as one of the standards for the third generation wireless system. Due to the use of nonconstant envelope modulation, the system has a stringent requirement on handset power amplifiers (PAs), demanding low distortion as well as high efficiency operation. PAs usually have to operate at a certain power backoff in order to satisfy the linearity requirement at the expense of reduced efficiency [1], [2]. In addition, the implementation of power control scheme in W-CDMA system requires variable gain amplifiers (VGAs) with wide control range and high linearity. However, conventional VGA design usually experiences re-growth on adjacent channel leakage power ratio (ACPR) when VGAs attenuation level increases, particularly in the intermediate attenuation range [3]. The cause is attributed to the nonlinearity associated with the devices used in the attenuators.

To address these issues, this paper investigates the use of amplifier linearization to overcome the problems. The design and fabrication of a complete PA block with power control ability is first presented. The block was obtained by cascading a linearized VGA and a two-stage PA MMICs. The linearized VGA, integrating a predistorter (PD) into a conventional VGA design, performs dual functions: to improve the linearity and efficiency of the following stage PA under high-power output, and to reduce distortion generated by the (conventional) VGA under power control operation. The power performance of the PA block under W-CDMA criteria is discussed. The linearity improvement over wide dynamic range under power control operation is also detailed.

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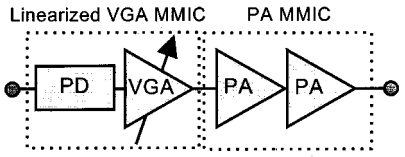

Fig. 1. Configuration of a power control W-CDMA PA block including a linearized VGA and a two-stage PA.

II. MMICs Design

The block diagram of the proposed power control W-CDMA PA is shown Fig. 1, consisting of a linearized VGA and a two-stage PA connected in cascade. The linearized VGA contains a PD and a conventional VGA, including an attenuator and an amplifier. The PD was designed to have inverse gain and phase responses to that of the VGA and PA for compensating the nonlinear gain and phase characteristics.

Fig. 2 shows the detailed implementation of the linearized VGA and PA MMICs. The active devices used are heterojunction FET (HJFET) which has shown excellent efficiency and linearity for W-CDMA application [4]. The linearized VGA consists of a PD, and a variable attenuator and a single-stage amplifier. The PD employs a common gate HJFET biased near pinchoff mode as a nonlinear generator [5], and was designed to have gain expansion and negative phase deviation characteristics with an increase in input power. The pair of shunt inductors were used to ensure the negative phase response [5]. The responses of the PD can be adjusted by the control voltage (V_{pd}) in order to compensate various nonlinearities of the VGA and PA under different attenuation and input power level. Following the PD is a variable attenuator, using a common gate configuration with a control voltage V_c used for adjusting the attenuation level, and a single-stage amplifier. The input and output matching circuits of the amplifier consist of LC matching networks. The linearized VGA was matched to 50 Ω input and output. Except for the drain bias circuit, all the elements of the VGA were realized on-chip shown inside the dash box.

The PA employs a two-stage design. Except for the output matching and drain biasing circuits, all other components, including input and inter-stage matching, were realized on chip which are enclosed in the dash box in Fig. 2. The output

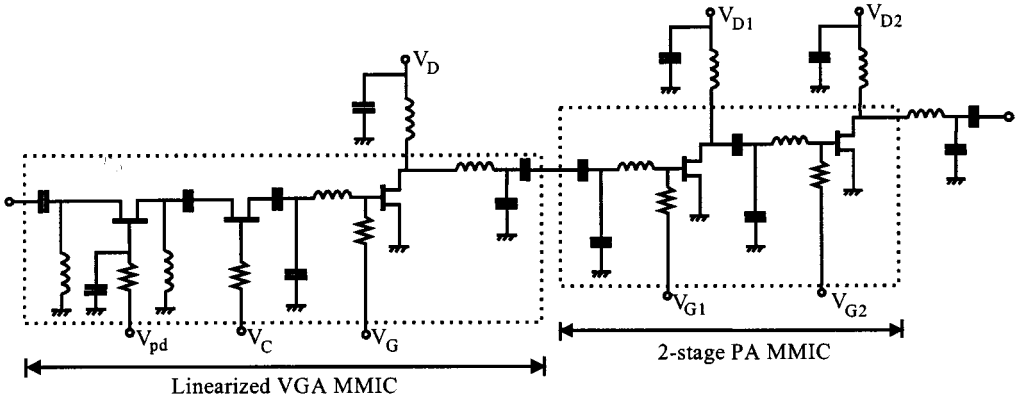

Fig. 2. Schematic of the PA block with a linearized VGA and a two-stage PA.

matching circuit was realized off-chip in order to reduce power loss which would have significantly effect on the overall efficiency.

Figs. 3(a) and (b) show the microphotographs of the fabricated VGA and PA MMICs, respectively. $SrTiO_3$ capacitors were employed for shrinking the size of the MMIC chip compared with the use of SiN_x-based capacitors. The chip sizes of the VGA and PA are 1.5×0.8 mm^2 and 1.6×1.6 mm^2, respectively.

III. Measured Results

The performance of the MMICs were evaluated using hybrid phase shift keying (HPSK) modulated signal with a chip rate of 3.84 Mcps at 1.95 GHz. The drain bias voltage (V_D and $V_{D1,2}$) of the amplifiers was set equal to 3.5 V. The amplifier in the VGA was biased at Class A in order to maintain good linearity at the output whereas the PA was biased under Class AB for high efficiency operation. V_{pd} and V_c were tuned to the required nonlinearity compensation and attenuation levels, respectively.

The performance of the PA block was measured by cascading the two MMICs similar to the block diagram shown in Fig. 2. The output matching circuit of the PA was tuned for optimum efficiency and linearity under W-CDMA criteria. Fig. 4 compares the W-CDMA power performance of the PA block with and without the use of PD. The case without PD was obtained by turning off the PD in the VGA by setting V_{pd} equal to 0 V. After the use of PD, the output power (P_{out}) and power added efficiency (PAE) of the PA block improved from 27.5 dBm and 39.8% to 28.5 dBm and 44.8%, respectively, measured at -35 dBc ACPR. The significant improvement on PAE is attributed to the improved gain linearity after the use of PD, reducing the ACPR level. The linearized VGA and PA MMICs showed a gain of 26.4 dB which is 3 dB lower than the case without PD. The lower gain is due to the gain loss of the PD. One added advantage of this configuration over integrating the PD into the PA [5] is that it can be easily applied to linearize any PA without significantly degrading PAE as well as gain.

Fig. 5 shows the power control characteristic of the PA block as a function of V_c for a fixed input power (P_{in}) of -2.3 dBm. By lowering V_c, the attenuation level increases, reducing the gain of the PA block. With the use of PD, the gain control range improved from 23.6 dB to 31.2 dB, achieving more than 7 dB improvement owing to the extra attenuation provided by the PD. It can be seen that ACPR increases sharply over the mid-attenuation level without the use of PD. At around -1 V V_c, ACPR is

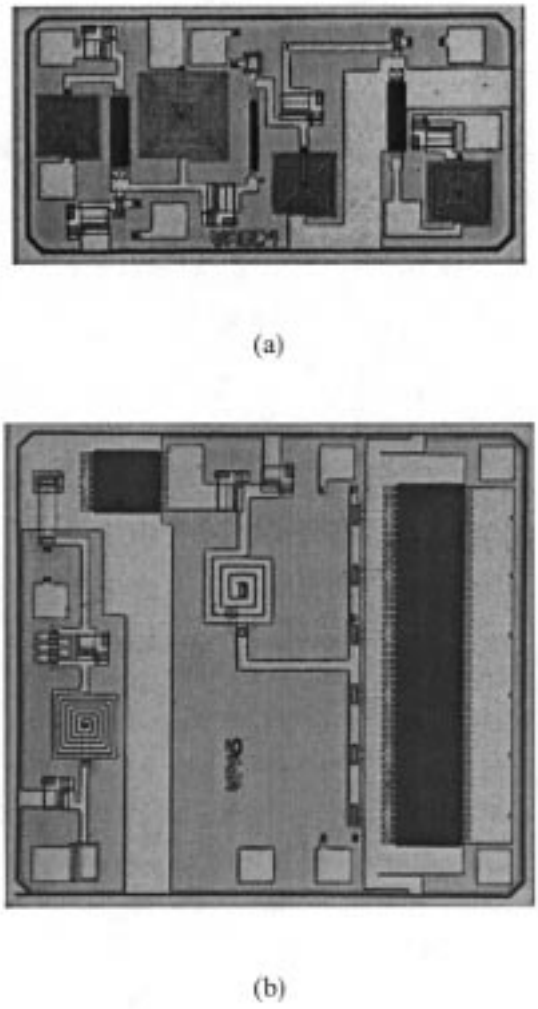

Fig. 3. Microphotographs of (a) linearized VGA and (b) PA MMICs.

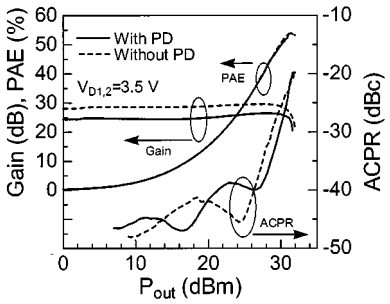

Fig. 4. Measured power performance of the PA block with and without PD.

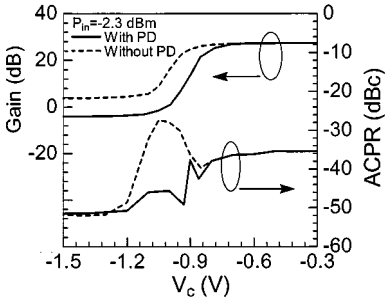

Fig. 5. Measured power control characteristics of the PA block with and without PD.

well above −35 dBc which fails to satisfy the linearity requirement of the PA. This effect is attributed to the nonlinearity associated with the HJFET used in the attenuator [3]. After the application of PD, however, significant reduction in ACPR level is obtained and is kept below the −35 dBc criteria over the whole attenuation range, with a maximum ACPR reduction of more than 10 dB. This characteristic is important for preserving the purity of the signal to satisfy the output linearity requirement.

IV. Conclusion

A linearized VGA and a two-stage PA MMICs were developed for 1.95 GHz W-CDMA handsets application. The linearized VGA consists of a PD integrated with a conventional VGA, performing dual function for achieving high linearity power control, as well as reducing output distortion level of the following PA MMIC. The complete PA block with power control ability was obtained by cascading the linearized VGA and the PA MMICs. With linearization, the $P_{\rm out}$ and PAE of the PA block improved from 27.5 dBm and 39.8% to 28.5 dBm and 44.8%, respectively, measured at −35 dBc ACPR. The power control range of the PA chain improved from 23.6 dB to 31.2 dB after the use of predistortion linearization on the VGA. ACPR reduction of over 10 dB was achieved over a wide range of control power. These characteristics are essential for wide dynamic power control range, high efficiency operation for W-CDMA handset PAs.

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